

Please add the following claims:

31. A method of storing data for use by an automated logic circuit design system comprising the steps of:
- providing a common database that allows for storage of data associated with automated circuit design; and
 - performing at least one logical operation and at least one physical operation, with each operation accessing the common database and modifying the data therein, the at least one logical operation including at least one of logic synthesis and timing simulation operations and the at least one physical operation including at least one of physical placement and physical routing operations.
32. The method according to claim 31 wherein each of the logic synthesis, timing simulation, physical placement, and physical routing operations are performed and each operation accesses the common database and modifies the data stored therein.
33. The method according to claim 31, wherein the at least one logical operation and the at least one physical operation is performed without translating circuit descriptions for usage by different design tools.
34. The method according to claim 33 wherein each of the logic synthesis, timing simulation, physical placement, and physical routing operations are performed and each operation accesses the common database and modifies the data stored therein.
35. The method according to claim 34 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the logical operation and another one of the plurality of area queries taking place during the at least one physical operation.
36. The method according to claim 33 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the logical operation and another one of the plurality of area queries taking place during the at least one physical operation.

37. The method according to claim 31 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the logical operation and another one of the plurality of area queries taking place during the at least one physical operation.

38. The method according to claim 1, wherein the steps of causing are performed without translating circuit descriptions for usage by different design tools.

39. The method according to claim 38 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the step of causing the computer system to synthesize logic elements and another one of the plurality of area queries taking place during the step of causing the computer system to generate physical placement information.

A2
Cnt
40. The method according to claim 1 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the step of causing the computer system to synthesize logic elements and another one of the plurality of area queries taking place during the step of causing the computer system to generate physical placement information.

41. A method of storing data for use by an automated logic circuit design system comprising the steps of:

providing a common database that allows for storage of data associated with automated circuit design; and

performing a plurality of different operations, each of which access the common database and modify the data therein, the plurality of different operations including at least three of logic synthesis, timing simulation, physical placement, and physical routing operations.

42. The method according to claim 41, wherein the at least three operations are performed without translating circuit descriptions for usage by different design tools.

43. The method according to claim 42 wherein each of the at least three operations are performed and each operation accesses the common database and modifies the data stored therein.

44. The method according to claim 43 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the logical operation and another one of the plurality of area queries taking place during the at least one physical operation.
45. The method according to claim 42 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the logical operation and another one of the plurality of area queries taking place during the at least one physical operation
46. The method according to claim 41 further including the steps of making a plurality of area queries, with one of the plurality of area queries taking place after the logical operation and another one of the area queries taking place during the at least one physical operation.
47. The method according to claim 41 further comprising the steps of:
making a copy of the data model; and
using the copy to formally validate a digital circuit.
-